REMARKS

Claims 1 through 12 are pending in the present application. Claims 1, 6, 10 and 11 have been amended.

The Office Action dated November 6, 2002, rejected claims 1, 6 and 10 under 35 U.S.C. 112, second paragraph, as being indefinite. The Action also rejected claims 1 to 4 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,759,610 to Yanagisawa ("the Yanagisawa patent"). In addition, claims 5 to 12 were rejected under 35 U.S.C. 103(a) as being as being unpatentable over the Yanagisawa patent in view of U.S. Patent No. 5,734,449 to Jang ("the Jang patent").

Regarding claim 1, it is respectfully submitted that present claim 1 is patentable over each of the cited references (i.e., the Yanagisawa patent and the Jang patent), and that claim 1 defines an invention that is neither disclosed nor suggested by the cited references and/or any proper combination thereof.

The Yanagisawa patent discloses an electrically conductive light shielding layer (28) formed on a transparent insulating substrate (16) so as to cover a TFT region before forming a TFT (11), a display pixel electrode (12) and a connecting portion (10). The Yanagisawa patent suggests that a silicon nitride film (29) serving as an insulating film be formed on the light shielding layer (28), that the TFT (11) and the display pixel electrode (12) be formed on the light shielding layer (28), and moreover, that the light shielding layer (28) be formed to overlap a part of the display pixel electrode (12) to form a supplemental storage capacitor. (col. 3, lines 41-49 and 59-63).

It is respectfully submitted that the above-described TFT arrangement differs from the transistor arrangement defined by present claim 1. Claim 1 has "substantially coplanar source and drain regions on [a] substrate" (emphasis added). Whereas, the Yanagisawa patent specifically teaches that source electrode (21) and drain electrode (20) be on insulator film (29), which is on light shielding layer (28), which in turn is on substrate (16). Thus, the source/drain arrangement of claim 1 is not disclosed or suggested by the Yanagisawa patent.

In addition, it is respectfully submitted that, contrary to that which was suggested by the Action, the Yanagisawa patent at least fails to disclose or suggest "a capacitor associated with said transistor and lying adjacent thereto." (emphasis added). In contrast, the Yanagisawa patent teaches that the light shielding layer is integral to both the TFT portion and the supplemental storage capacitor. (col. 2, lines 62-68); (Fig. 7). Hence, it is respectfully submitted that the TFT/capacitor arrangement as disclosed/suggested by the Yanagisawa patent is clearly different from that of present claim 1. Accordingly, the Yanagisawa patent fails to disclose all of the features defined by defined by claim 1. Thus, reconsideration and withdrawal of the rejection, and allowance of claim 1 are respectfully requested.

Regarding claims 2 to 5, which depend either directly or indirectly from claim 1, it is respectfully submitted that they are each patentable at least for the reasons discussed above with respect to claim 1. Accordingly, reconsideration and withdrawal of the rejection, and allowance of claims 2 to 5, are respectfully requested.

Regarding claim 6, it is respectfully submitted that claim 6 is patentable over the cited combination of the Yanagisawa patent with the Jang patent at least for the reasons discussed above with respect to claim 1. It is further respectfully submitted that claims 7 to 9, which depend either directly or indirectly from claim 6, are likewise patentable at least for the reasons stated above with respect to claim 1.

Regarding claim 10, as with claim 6, it is respectfully submitted that claim 10 is patentable over the cited combination of the Yanagisawa patent with the Jang patent at least for the reasons discussed above with respect to claim 1. It is further respectfully submitted that claims 11 and 12, which depend either directly or indirectly from claim 10, are likewise patentable at least for those reasons stated above with respect to claim 1.

In sum, it is respectfully submitted that the present pending claims are clearly patentable over each of the cited references and/or any proper combination thereof. Thus, this application is in condition for allowance. Accordingly, reconsideration and withdrawal of all rejections of the claims are respectfully requested.

Dated: 1/23/2003

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend claims 1, 6, 10 and 11 as follows:

1. (Amended) A transistor substrate for a liquid crystal display comprising:

a substrate;

a transistor over [the] said substrate, [the] said transistor [comprising] having an insulated-gate staggered structure [having] with substantially coplanar source and drain regions on said substrate, [and] a gate region, and a gate insulator lying between [the] said gate region and [the] said source and drain regions; and

a capacitor associated with [the] said transistor and lying adjacent [the transistor] thereto, [the] said capacitor [comprising] having a stacked structure of two electrodes separated by a capacitor dielectric,

wherein [the] said gate [insulator comprises] region has a first inorganic layer and a second, polymer or spin-on glass layer, of which layers only the polymer or spin-on glass layer extends to [the] said capacitor to define [the] said capacitor dielectric.

6. (Amended) A liquid crystal display comprising:

a plurality of pixels each [comprising] having a switching

transistor, a storage capacitor of capacitance C_{store}, and liquid crystal material of capacitance C_{LC}, [the] said transistors [comprising] having insulated-gate staggered structures [having] with substantially coplanar source and drain regions on said substrate, [and] a gate region, and a gate insulator lying between [the] said gate region and [the] said source and drain regions, [the] said capacitor [comprising] having a stacked structure of two electrodes separated by a capacitor dielectric,

wherein [the] said gate [insulator comprises] region has first and second layers, of which layers only the second extends to [the] said capacitor to define [the] said capacitor dielectric, and wherein the thicknesses of [the] said first and second layers are selected such that the charging time constant of each pixel is invariable to first order changes in the thickness of second layer defining the capacitor dielectric.

10. (Amended) A method of manufacturing a transistor substrate for a liquid crystal display, comprising providing an array of transistors and capacitors over the substrate, [the] said transistors [comprising] having insulated-gate staggered structures [having] with substantially coplanar source and drain regions on said substrate, [and] a gate region, and a gate insulator lying between [the] said gate region and [the] said source and drain regions; and [the] said capacitors [comprising] having a stacked structure of two electrodes separated by a capacitor dielectric,

wherein [the] said gate [insulator] region is deposited as first and second layers, a first layer being deposited by vacuum deposition process, and a second layer being deposited by a non-vacuum process, [the] said first layer being patterned to remove

it from areas corresponding to [the] said capacitors, and [the] said second layer extending to the areas corresponding to [the] said capacitors to define [the] said capacitor dielectric.

11. (Amended) A method of manufacturing a liquid crystal display, comprising manufacturing a transistor substrate using the method of claim [8] 10, and providing liquid crystal material over [the] said transistor substrate,

wherein [the] said first [insulator] layer is deposited to a thickness d_1, and [the] said second layer is deposited to a thickness d_2, the thicknesses being selected such that the charging time constant of each pixel is invariable to first order changes in the thickness of second layer defining the capacitor dielectric.

NEWLY ADDED CLAIMS

13. (Newly added) A transistor substrate as claimed in claim 1, wherein said gate insulator and said first inorganic layer are patterned using the same mask to define a semiconductor island forming a transistor body.

2871

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Stephen J. Battersby et al.

Serial No.: 09/728,189

For: LIQUID CRYSTAL DISPLAY AND METHOD OF MANUFACTURE

Filed: December 01, 2000

Examiner: Akkapeddi, Prasad R.

Group Art Unit: 2871

Attorney Docket No.: PHB 34,424

Commissioner for Patents
Washington, D.C. 20231

AMENDMENT TRANSMITTAL FORM

Dear Sir:

XX Transmitted herewith is an Amendment Response in the above-identified application, a transmittal in duplicate and a potstcard.

_____ Petition for a one month extension of time pursuant to 37 C.F.R. §§ 1.136 and 1.137 is hereby made if, and to the extent, required. The fee for this extension of time is calculated to be $____ to extend the time for filing this response until _____.

The fee for any change in number of claims has been calculated as shown below.

CLAIMS AS AMENDED						
	Claims Remaining After Amendment		Highest Number Previously Paid	Present Extra	Rate	
Total Claims	13	Minus	20	0	0 X $18.00	$0.00
Independent Claims	3	Minus	3	0	0 X $84.00	$0.00
MULTIPLE DEPENDENT CLAIM FEE					x $270.00 =	$
TOTAL FEE FOR CLAIM CHANGES						$0.00

The total fee for this amendment is calculated to be $____.

_____ A check in the amount of $ **0.00** _____ is attached.

The Commissioner is hereby authorized to charge any additional fees under 37 C.F.R. §§1.16 and 1.17 which may be required with this communication or during the entire pendency of the application, or credit any overpayment, to **Deposit Account No. 01-0467**. A duplicate copy of this Form is enclosed.

January 24, 2003
Date

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CERTIFICATE OF MAILING

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO: COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231, ON January 24, 2003.

DAVID L. BARNES
NAME

SIGNATURE

1/24/03.
DATE